THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD L. SITES and RICHARD T. WITEK

Appeal No. 1997-0586
Application 08/243,559

ON BRIEF

Before LALL, DIXON and GROSS, Administrative Patent Judges.

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection[1] of claims 1 to

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[1] An amendment after the final rejection was filed [paper no. 21], however, no changes to the claims were made.

20, which constitute all the claims in the application.

The disclosed invention relates to a pipelined processor having a plurality of registers. Jump instructions in such a processor in the prior art cause a delay in pipeline processing because the target address for a jump instruction may not be readily available. The invention creates a jump instruction which has the target instruction address and a predicted address as a part of the instruction itself so that these two addresses are readily available, thus substantially eliminating the delay of fetching these addresses from elsewhere in the processor system. Thus, a jump instruction for this processor includes an opcode, a register specifier and a memory address specifier. A first address, which is the target address of a jump instruction, is extracted from said register specifier. A second address, which is a prediction of said target address, is extracted from said memory address. The invention is further illustrated by the following claim.

1. A method of operating a pipelined processor, said processor having a plurality of registers in a register set, and having a program counter for counting sequential addresses in memory, comprising the steps of:

fetching instructions from said sequential addresses

in memory using said program counter, and decoding said instructions before executing said instructions,

detecting a jump instruction in the fetched instructions, said jump instruction including an opcode, a register specifier and a memory address specifier, and extracting from said register specifier of said jump instruction an identification of a first of said registers for storing a first address which is a target address of said jump instruction, and extracting from said memory address specifier of said jump instruction a second address which is a prediction of said target address; and

prefetching an instruction from said second address rather than from said sequential addresses, before said jump instruction is executed and before said first address is available in said first register.

The references relied on by the Examiner are:

Beckwith et al. (Beckwith)	5,136,696	Aug. 4, 1992 (Filed June 27, 1988)
Johnson	5,136,697	Aug. 4, 1992 (Filed Jun. 06, 1989)

Kane, Gerry (Kane), “MIPS R2000 RISC ARCHITECTURE”, Prentice Hall, Englewood Cliffs, NJ, 1987, pages 1-1 to 4-11 and A-1 to 1-9.

Claims 1 and 14 stand rejected under 35 U.S.C. § 103 over Beckwith and Johnson, while 2 to 13 and 15 to 20 stand rejected over Beckwith, Johnson and Kane.

Reference is made to Appellants' briefs and the Examiner's answers for their respective positions[2].

OPINION

We have considered the record before us, and we will reverse the rejections of claims 1 to 20.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459,

[2] A reply brief was filed as paper no. 27 to which the Examiner responded by a supplemental answer as paper no. 28.

467 (CCPA 1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S.
825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. System., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Furthermore, the Federal Circuit states that "[the] mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the

modification." In re Fitch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), citing In re Gordon, 773 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. V. SGS Importers Int'l, 73 F.3d 1087, 37 USPQ 2d at 1239 (Fed. Cir. 1995), citing W. L. Gore & Assocs., v. Garlock, Inc., 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13 (Fed. Cir. 1983).

Claims 1 and 14

These claims are rejected over Beckwith and Johnson. The Examiner recognizes [final rejection, page 2] that "Beckwith et al. do not teach the branch instruction including an opcode, a register specifier, and memory address specifier." The Examiner contends that Johnson "taught the branch instruction including a branch prediction target address" [id. 2 and 3]. The Examiner points to the abstract of Johnson for this teaching. The Examiner then asserts [id. 3] that "it would have been obvious ... to incorporate the teaching of

Johnson into [sic] system taught by Beckwith et al. ... by including the prediction target address at the branch instruction level, thereby processing the branch instruction without waiting for a decoder or execution unit to indicate the proper fetched action to be taken for correctly predicted branching."

Appellants argue [brief, page 11] that "the abstract and disclosure of Johnson as a whole teach that the branch prediction information of Johnson is stored in a cache block of instruction cache memory, and not in a field of the branch instruction. Johnson fails to disclose or suggest a branch instruction specifying a prediction of the target address in addition to a register specifier for the actual target address."

We have also reviewed appellants' further arguments [brief, pages 12 to 17 and reply brief, pages 2 to 4] and the Examiner's responses thereto [answer, pages 3 to 8 and supplemental answer, pages 1 to 3] and are of the view that Johnson does not provide the teaching suggested by the Examiner. In fact, the Examiner "agrees with appellant's [sic, Appellants'] argument that Johnson et al [sic, et al.]

did not teach that an instruction contains a predicted address within the instruction. However, Johnson et al [sic et al.] taught that each instruction block contains a plurality of instructions and instruction fetch information." [Answer, page 7]. It is clear that Johnson has to go to the cache memory which contains instruction blocks, and each instruction block contains a plurality of instructions and instruction fetch information. Thus, a jump instruction in Johnson does not have the predicted address as a part of the instruction, but instead has to go the cache memory to obtain it.

Therefore, we do not sustain the obviousness rejection of claim 1 and claim 14 over Beckwith and Johnson, as each claim contains the recitation discussed above.

Claims 2 to 13 and 15 to 20

These claims are rejected over Beckwith, Johnson and Kane. Each of these claims also contains at least the recitation discussed above. The Examiner asserts [final rejection, pages
3 to 4] that Kane "taught that the instructions are of fixed length" and Kane also shows "an address of the first register [RD] in which is stored the first address which is the target

for loading the program counter when jump instruction is executed;" and "a displacement field [RT] which contains the second address and is otherwise not necessary [sic] used upon execution." Appellants argue [brief, pages 20 to 21], and we agree, that "the jump instruction disclosed in the Kane reference (at pages 3-1 to 3-16) does not provide any information other than an operation code and a jump target address. There is simply no suggestion in the Kane reference of how a prediction of the jump target address can be extracted from the jump instruction." [Id. 20]. (Emphasis added). Thus, we conclude that Kane does not cure the deficiency noted above with the combination of Beckwith and Johnson. Therefore, we do not sustain the obviousness rejection of these claims over Beckwith, Johnson and Kane.

In conclusion, the Examiner's decision rejecting claim 1 to 20 under 35 U.S.C. § 103 is reversed.

REVERSED

PARSHOTAM S. LALL Administrative Patent Judge	)	
JOSEPH L. DIXON Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ANITA PELLMAN GROSS Administrative Patent Judge	)	

PL/dm

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